# Design and Simulation of Second Order Type-II Phase Locked Loop

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**Abstract: This paper presents the design, analysis and simulation of a third order, type-II charge pump PLL. The designed system includes a current-starved ring oscillator with 16 MHz centre frequency, dissipating an average power of 100uW, a phase-frequency detector, a low-current charge pump and a loop-filter. The PLL has fine stability margins (Phase margin: $50^0$, Gain Margin: 28 dB) transient characteristics (15 u sec settling time) and a wide lock range of 22 Mhz.**

**Keywords: Oscillator, Phase-Frequency Detector, Low-current Charge Pump and Stability Margin.**

## I. INTRODUCTION

Phase-Locked Loop (PLL) is an important block of Analog and Mixed Signal systems. The improvements in integrated circuit technology and analog design techniques for low power have produced increasingly efficient and reliable PLLs. A basic second-order PLL fails to meet such ever-growing demands and is less suitable for IC realization.

The third-order charge pump PLL architecture presented in this paper has been widely used over basic PLL architecture. **The paper presents a study of a complex third order feedback system, with challenging stability issues**. A linearized phase-domain model, for evaluating the stability of the PLL has been constructed. **The designed PLL can be used in several applications such as frequency multipliers, FM demodulators etc**.

Charge pump PLL, presented in the paper, uses a synchronous phase-frequency detector that aids the system to track both phase and frequency of the input. The phase-frequency detector responds to both phase and frequency difference between the signals and thus aids the PLL to acquire lock. The capture range and lock range of the charge pump PLL is largely superior to those of basic second order PLL with an XOR phase detector. The charge pump PLL, due to the wider operating range of synchronous phase-frequency detector has an improved lock-range, zero steady-state error when the loop is locked owing to infinite DC gain, and is insensitive to duty-cycle of input because of the synchronous PFD.

## II. SYSTEM AND IC ARCHITECTURE

The figure shows the top-level architecture of the system. It consists of a synchronous phase-frequency detector, a charge pump, loop filter and a voltage-controlled oscillator.

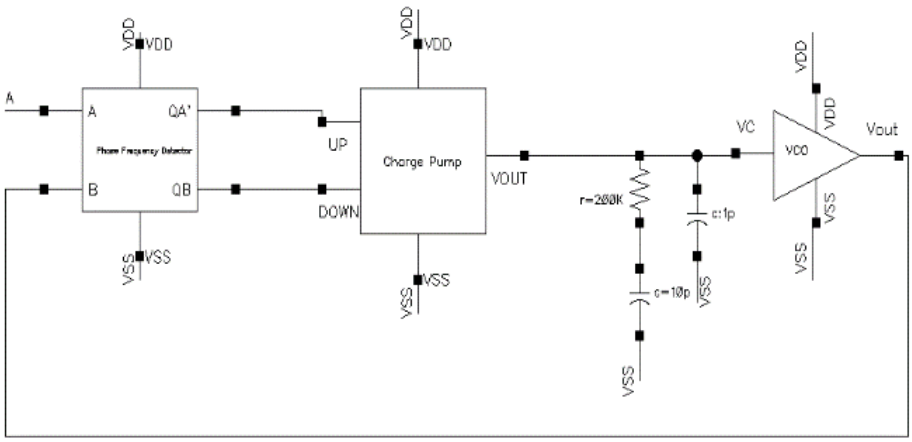


**Figure 1 - Top Level Architecture**

Although the second order PLL is always stable, there is a trade-off between various performance parameters. Its performance is quite limited in terms of parameters such as lock range and capture range.[2]-[5] The phenomenon of lock acquisition is largely non-linear. If the frequency of input is very far from that of output, the loop will not lock. The cut-off frequency of loop-filter is an essential parameter for it governs the overall behavior of the system [2].Usually the cut-off frequency is chosen to be lower than the crossover frequency of PLL for attenuating ripples on VCO control line. This leads to unacceptable value of phase margin.[4]

The implemented charge-pump PLL overcomes all these shortcomings and has thus been widely implemented in IC technology.

The entire circuit design along with sub-blocks is done using the Cadence Virtuoso(R) Schematic Editor L Version 6.1.5. The different blocks include synchronous phase-frequency detector, charge pump, loop filter and voltage-controlled oscillator. The system simulations are done using Cadence Virtuoso (R) Analog Design Environment XL.

A linearized model is constructed for evaluation of stability of the loop and the transient performance of the loop. Various performance parameters of the loop such as lock-range, and settling time are evaluated using appropriate test-benches.

## III. ELECTRICAL DESIGN METHODOLOGY

This section presents the description and architecture of all the sub-blocks, along with their simulated performance results.

### Current-Starved Voltage Controlled Oscillator

A voltage-controlled oscillator is a circuit whose frequency of oscillation can be controlled by a voltage input. The applied control voltage determines the instantaneous frequency of oscillation. Figure shows the schematic of a current starved ring oscillator.

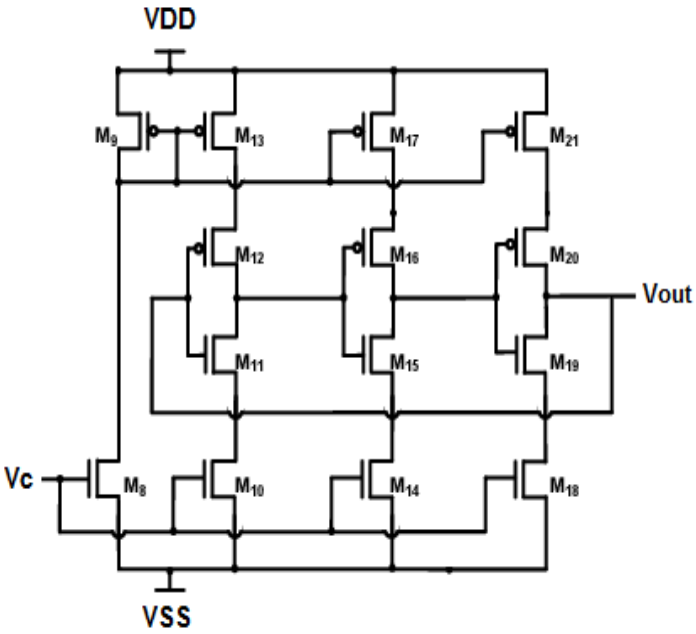


**Figure 2 - Current Starved Ring Oscillator**

In a current-starved Voltage Controlled Oscillator, a ring of inverters is fed with currents that alternately charge and discharge the effective capacitance of the subsequent stage [4]-[9]. The obvious advantage of this arrangement is its immunity to supply variations; as long as the current sources feeding the inverters continue to behave as current sources, the output frequency remains constant.[4] It is easy to exercise control over the oscillation frequency since, for a particular size of inverters' MOSFETs, the current fed to them determines the frequency. [9]

Figure shows the complete schematic of a current-starved Voltage Controlled Oscillator, with five stages.

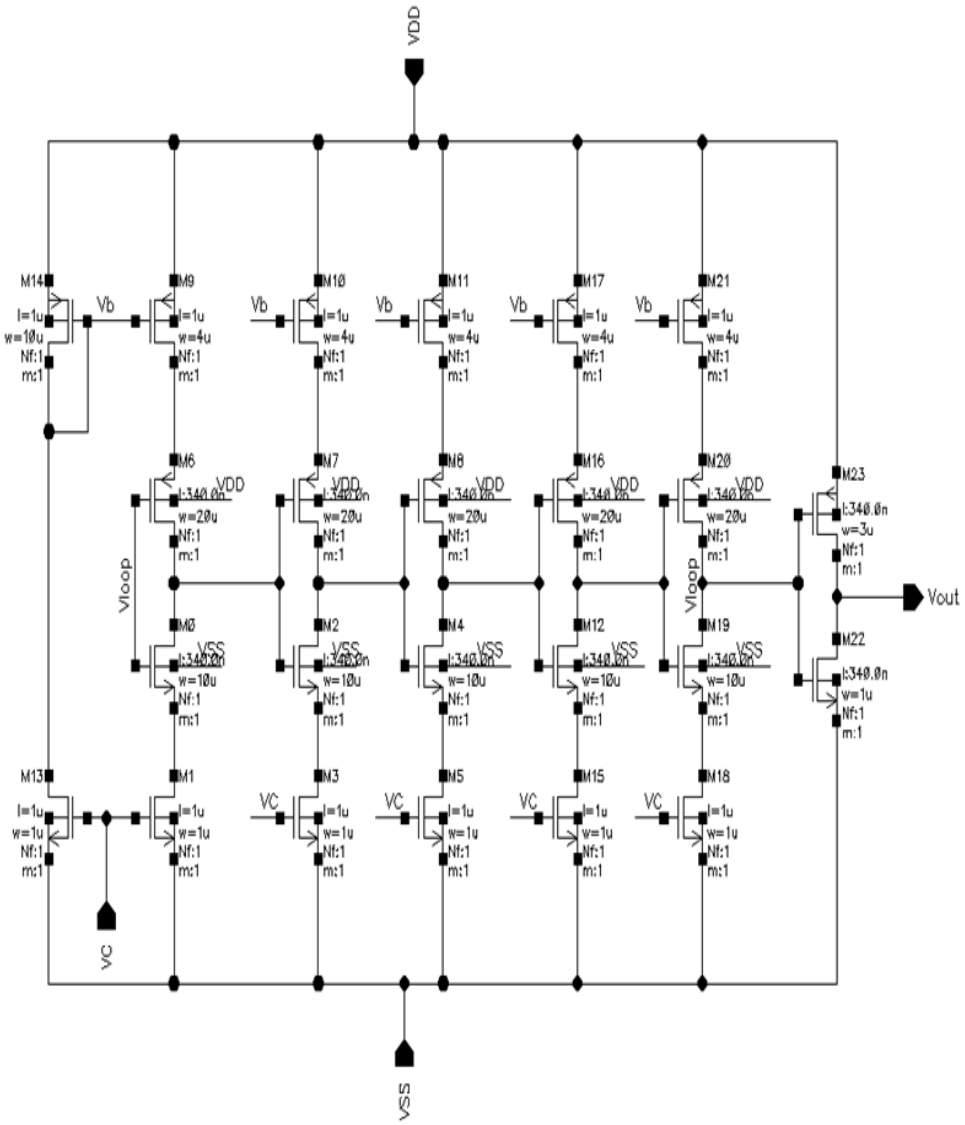


**Figure 3 - Current-Starved VCO with Five Stages.**

The dimensions of inverters are chosen such that PMOS and NMOS have equal drives. The size of inverters is (W)p = 10 um and (W)n = 20 um, (L)p = (L)n = 340 nm.

The effective capacitance, for the given size is found out to be 110 fF. For the centre current (when Vc = Vdd/2), the centre frequency of oscillation is 16 MHz

The simulated characteristics of Voltage Controlled Oscillator are as shown in the figure. The gain of the Voltage Controlled Oscillator, around the center frequency, as seen from the characteristic is nearly 20 MHz/V. Due to its inherent non-linearity, the gain is not constant throughout the range of operation. The gain of Voltage Controlled Oscillator essentially determines the overall loop gain of the system and hence affects many performance parameters.

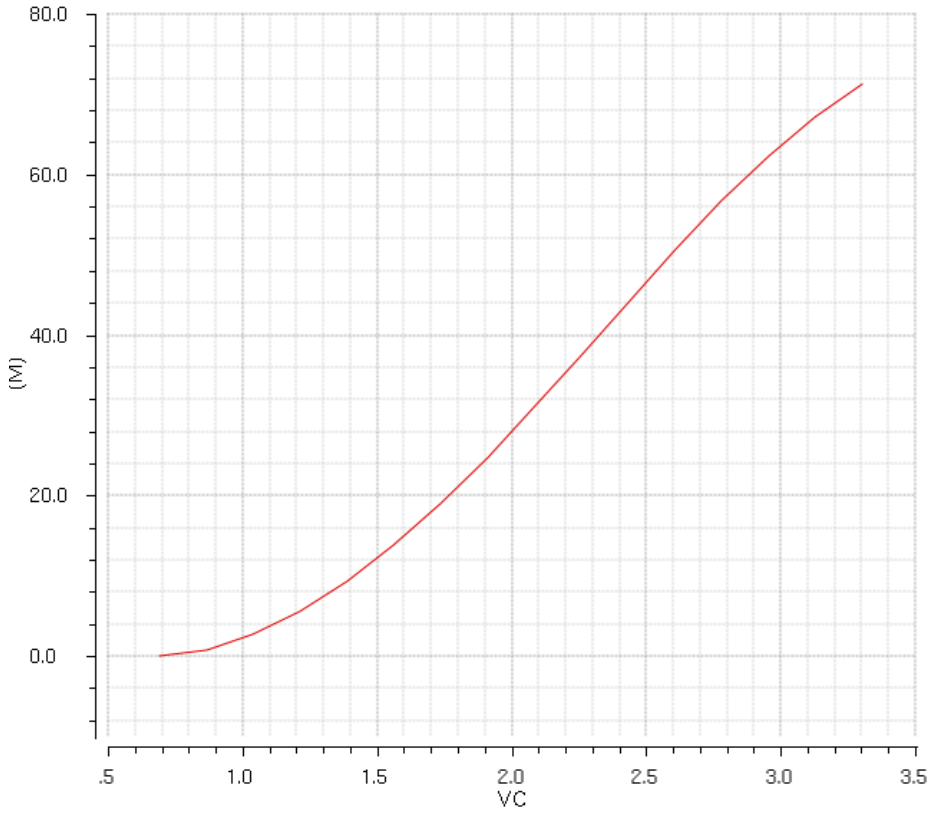


**Figure 4 - Characteristics of VCO**

## Phase-frequency detector (PFD)

In order to aid PLL in acquiring lock, a sequential logic can be employed. A PFD produces an output that depends both on frequency and phase differences between its inputs. A PFD relaxes the condition that output of VCO must have 50 percent duty cycle since it responds only to rising or falling edges of inputs [6]-[9].

The PFD described is implemented using edge-triggered D flip-flops [6]. PFD implementation along with the circuit's response to signals of different frequencies is as shown below:

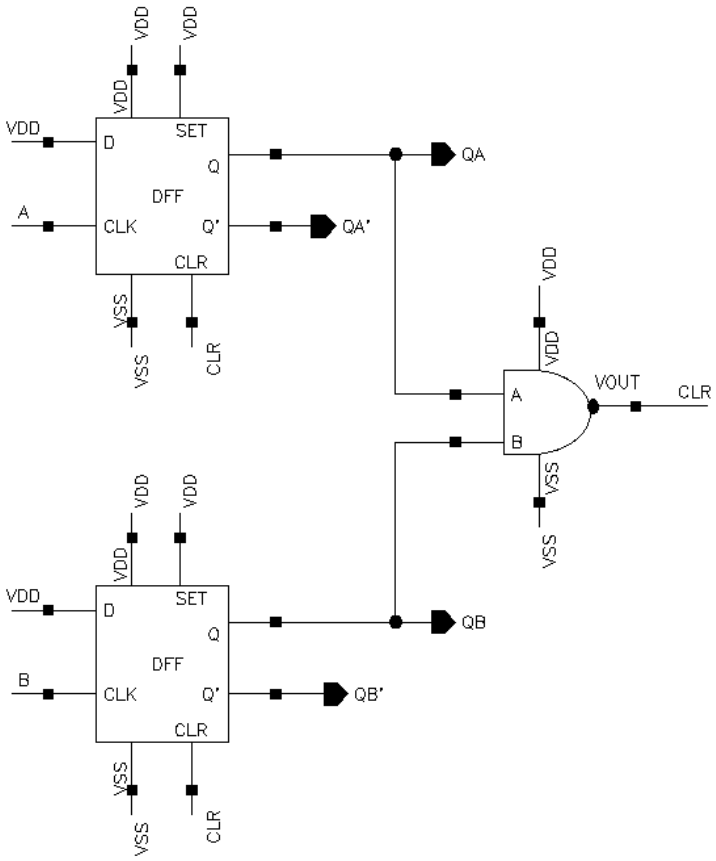


**Figure 5 - Phase-Frequency Detector**

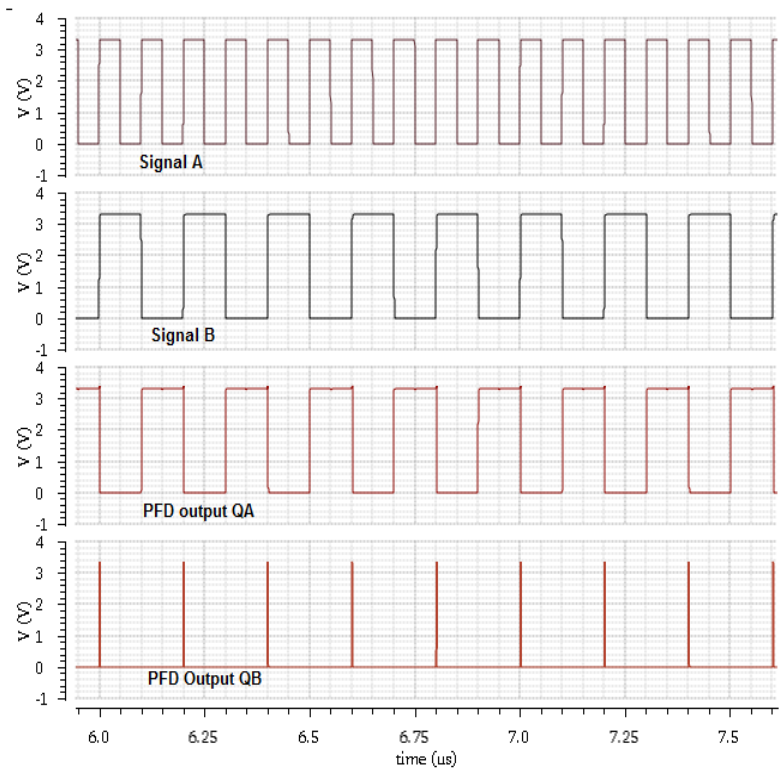


**Figure 6 - Characteristics of Phase-Frequency Detector**

**Charge pump and loop filter**

Charge pump PLLs are the most widely implemented PLL architectures. Charge pump converts the digital output of phase-frequency detector into its analog equivalent to control the loop. A charge pump consists of two switched constant current sources that feed charge into the loop filter as dictated by the input signals. The input signals to charge pump, called the UP and DOWN signals, are the outputs of PFD.The filter capacitor is charged or discharged, depending on the input signals. The output of loop filter acts as the control voltage to the VCO, changing its output frequency until the input reference signal and VCO output have exactly same frequency, and zero phase difference.

When the loop is in lock, the loop filter capacitor maintains its voltage, continuing the provide bias for the VCO. Any variation in the phase or frequency between the two inputs turns on the appropriate switch in the charge pump, because of which the output voltage of filter rises or falls. The figure shows the schematic of implemented charge-pump.

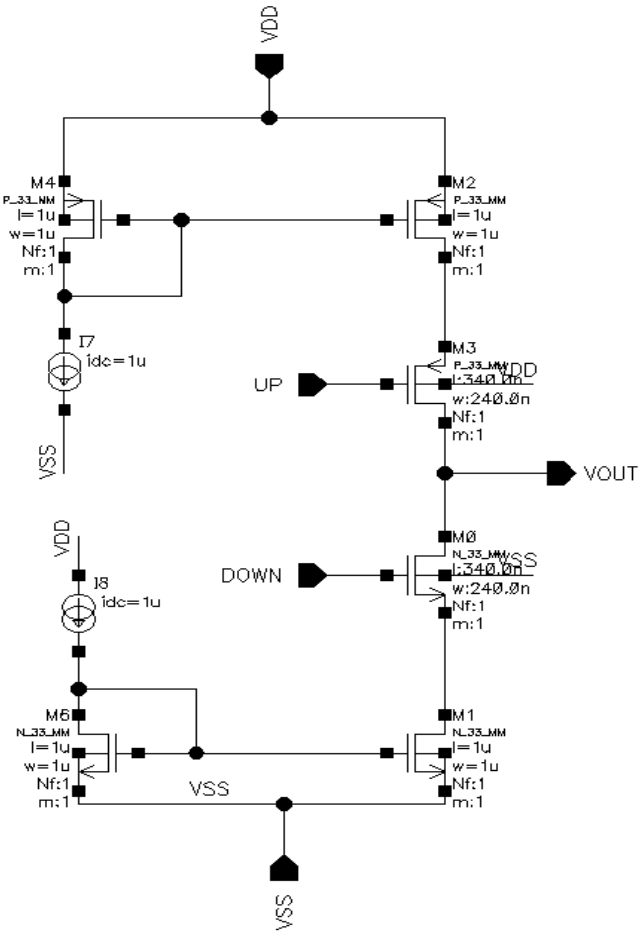


**Figure 7 - Charge-Pump**

Transistors M1 and M2 in the figure act as current sources, mirroring the reference current by a factor set by device dimensions. Transistors M0 and M3 are the switches controlled by the PFD outputs- UP and DOWN signals. The currents I1 and I2 are both 1uA. It is to be noted that, since the UP signal

drives a PMOS switch, it should be inverted so that transistor M3 turns on when UP signal is high. The complementary output of D flip-flop is thus used to drive M3 while the DOWN signal is used to control M0.

A charge pump PLL of second order, is a stable feedback loop with a zero in the transfer function. However, there is a significant problem of increased ripples on VCO control input. The PFD continuously produces pulses of varying width, controlling the switches of charge pump. Consequently, the loop filter capacitor is charged and discharged. However, the resistor in loop filter impedes the instantaneous charging or discharging of the capacitor and thus the filter output voltage exhibits severe ripple.

A third order PLL is hence designed to overcome this issue. A second order loop filter is used with an additional capacitor connected in parallel with series combination of R1 and C1.

The transfer function of the system reveals an additional pole, inevitably reducing the phase margin. The pole is always at a higher frequency compared to zero. It can be seen that if the loop-gain is increased, the phase margin worsens further. However, it is easy to stabilize the system by making the zero more dominant than pole. It must be ensured that the pole added by C2 lies far away from crossover frequency. C2 is made $1/10^{th}$ of C1, which ensures a good phase margin for the system.

The following figures show the lock transients- the control voltage and frequency of the output, in the process of acquiring lock. The settling time, measured when the frequency of output and reference are exactly equal, is found to be 17 us. The results are evaluated with an input pulse of 20 MHz frequency. As shown in the frequency transient curve, the output frequency exhibits transients and steadily reaches the value of 20MHz at 17 us.

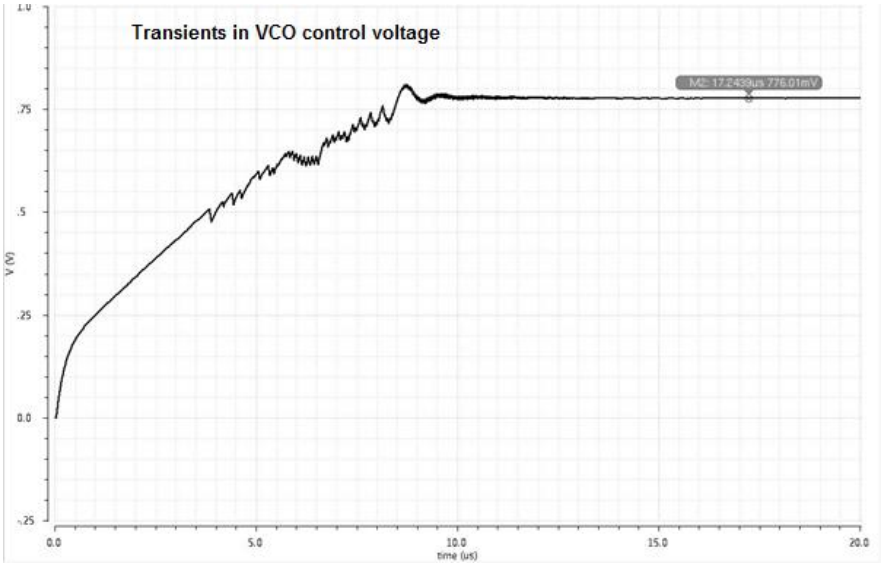


**Figure 8 - Frequency Transient Curve**

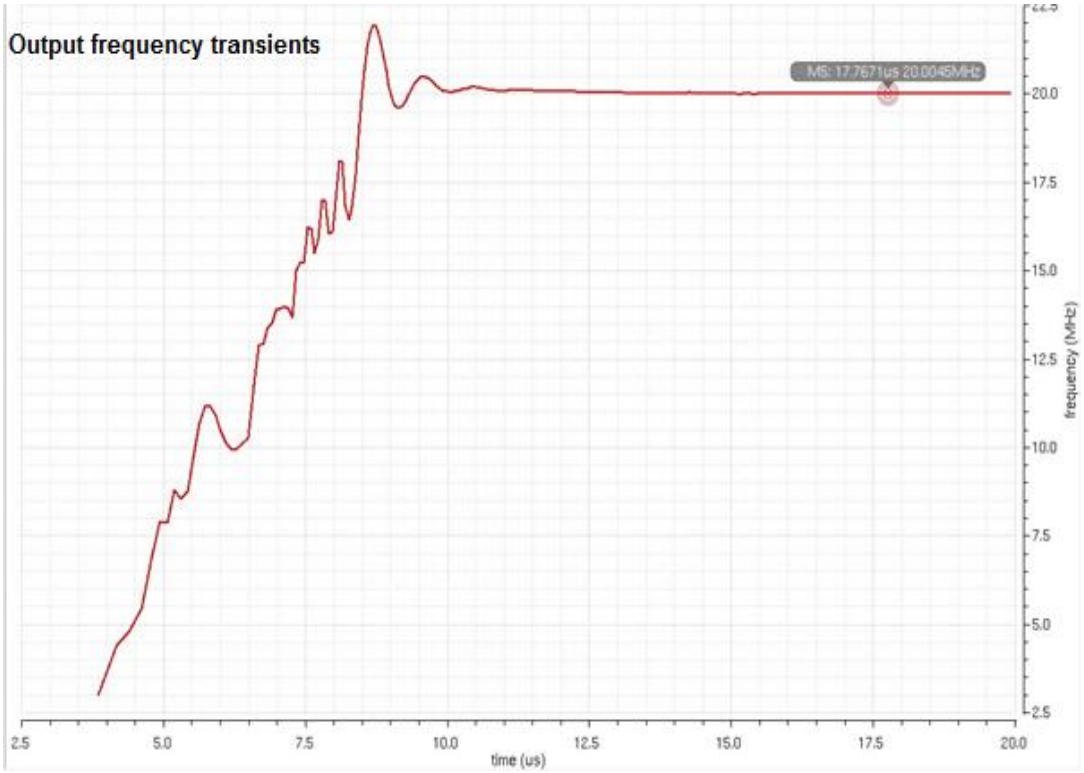


**Figure 9 - Output Characteristics**

The input and output signals when PLL is in lock, are as shown in the figure. Test bench for evaluating the transient parameters of system is same as the one shown in Fig. As can be seen in the result, under locked state, input and output are aligned and have exactly the same frequency.

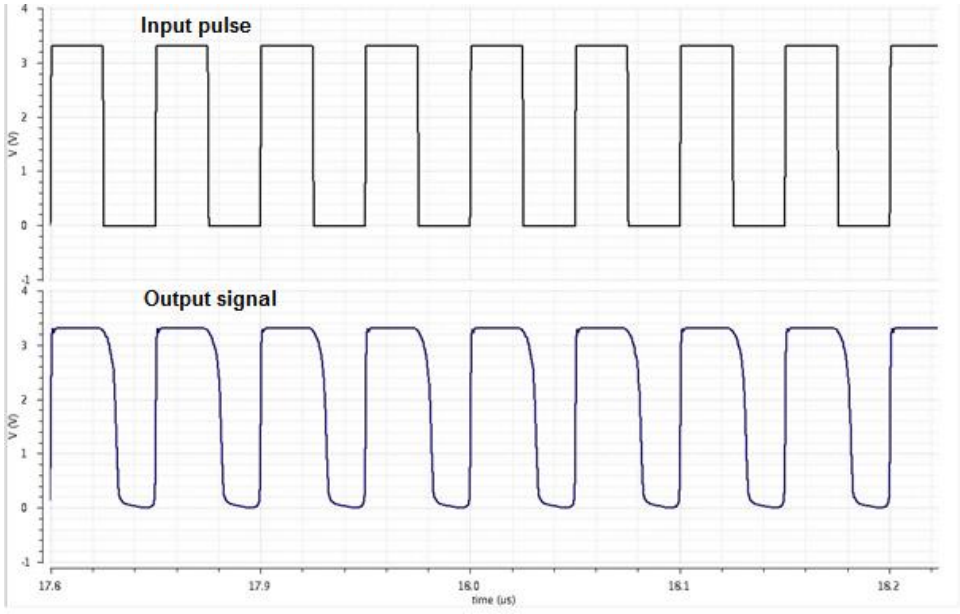


**Figure 10 - Input and Output Signal Compariison when PLL is in Lock**

The lock-range of PLL is a quantity of interest. Fig shows the simulated lock range of the designed PLL. The time-period of input signal is swept in a wide range of values once the PLL acquires lock, and the output time-period is plotted as a function of input time-period. The range under which the

curve is a straight line of unity slope, implying that the input and output have same frequencies, is the lock range of PLL. The lock-range of the PLL is 33 MHz, the center frequency being 16 MHz.

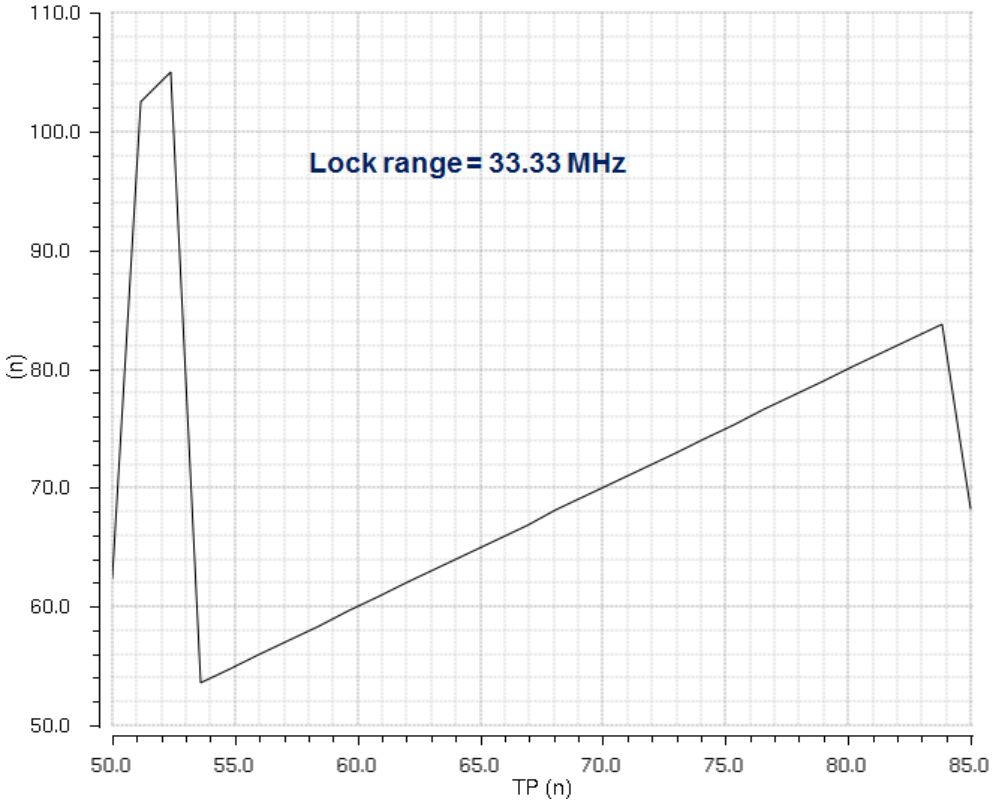


**Figure 11 Simulated Lock Range of the Designed PLL**

## IV. Conclusion

The designed third-order charge-pump PLL is a stable loop with phase margin of 50 degrees. One of the most challenging components to design, the charge pump, uses a current of 1uA. **The center frequency of the designed VCO is 16 MHz**.

The lock transients, as discussed in the results, require 17 us settling time. The input and output signals are perfectly aligned when the loop is locked. With 20 MHz, frequency input signal, as shown in results, the output tracks the input signal and attains exactly the same frequency. **The designed PLL has a lock range of 33 MHz**.

## V. Acknowledgment

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## VI. Full Forms

1. VCO – Voltage Controlled Oscillator
2. PFD – Phase-Frequency Detector

3. PLL – Phase Locked Loop

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